



## **J9152A-ECO**

# 10Gbps 220m Multi Mode Datacom SFP+ Transceiver

#### **Features**

- Supports 9.95 to 10.3Gbps bit rates
- Transmission distance up to 220m (OM1 fiber)
- Hot Pluggable SFP+ footprint
- 1310nm FP transmitter, PIN photo-detector
- Digital Status monitoring Interface
- Duplex LC connector
- RoHS compliant and Lead Free
- Metal enclosure for lower EMI
- Single 3.3V power supply
- Power dissipation < 1W</li>
- Operating case temperature: 0 to 70°C
- Compliant with FC-PI-4 800-Mx-SN-I, SFF-8431, SFF-8432 and SFF-8472

## **Applications**

- 10GBASE-LRM 10G Ethernet
- Legacy FDDI multimode links

# **Product description**

SFP+ LRM is an optical transceiver module for transmission at 1310nm over legacy multimode fiber. Supporting 10GBASE-LRM Ethernet standard make it ideally suited for 10G datacom. Its very low power consumption and its excellent EMI performance allow system design with high port density. The small form factor integrates a 1310nm Fabry-Perot (FP) laser in an LC package and a linear multimode PIN receiver. Module is lead free, RoHS compliant and is designed and tested in accordance with industry safety standards.



The J9152A SFP+ transceiver is a linear-interface transceiver that enables, in conjunction with an Electronic Dispersion Compensation (EDC) on the host board, an IEEE802.3aq 10GBASE-LRM compliant link. The host board EDC provides correction for the severe modal dispersion that may occur during propagation through multimode fiber links, including legacy installed FDDI multimode fiber (see IEEE802.3aq for detailed information regarding fiber coverage).

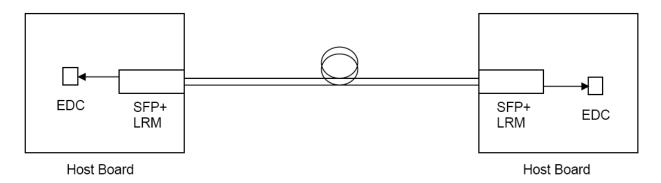


Figure 1. Block Diagram of SFP+ LRM Module on Host Board with EDC

Unlike the XFP MSA transceiver requirements, the SFP+ transceiver does not contain internal retiming circuitry, and thus some of the Transmitter Optical Characteristics stated in this data sheet require that the Host Board is compliant to the SFP+ MSA specifications. See Chapter 3 in Reference [1] for further details.

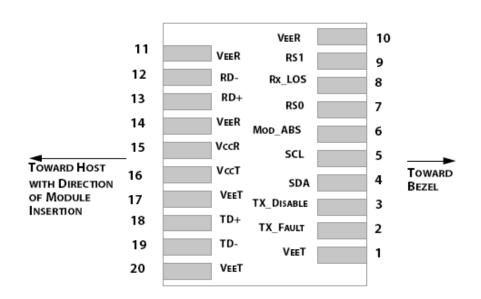
### Pin definition

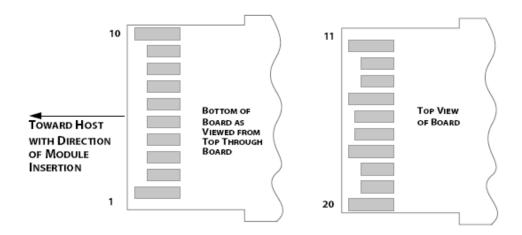
The SFP+ modules are hot-pluggable. Hot pluggable refers to plugging in or unplugging a module while the host board is powered. The SFP+ host connector is a 0.8 mm pitch 20 position right angle improved connector specified by SFF-8083, or stacked connector with equivalent with equivalent electrical performance. Host PCB contact assignment is shown in Figure 2 and contact definitions are given in Table 2.

SFP+ module contacts mates with the host in the order of ground, power, followed by signal as illustrated by Figure 3 and the contact sequence order listed in Table 2.



10GBASE-LRM SFP+, 1310nm, MMF, 220m, Dual LC, DOM for HP









Contacts	logic	Symbol	Power Sequence Order	Name/Description			
1		VeeT	1st	Module Transmitter Ground			
2	LVTTL-O	TX_Fault	3rd	Module Transmitter Fault			
3	LVTTL-I	TX_Disable	3rd	Transmitter Disable; Turns off transmitter laser output			
4	LVTTL- I/O	SDA	3rd	2-wire Serial Interface Data Line (Same as MOD-DEF2 in the INF-8074i)			
5	LVTTL- I/O	SCL	3rd	2-wire Serial Interface Clock (Same as MOD-DEF1 in the INF-8074i)			
6		Mod_ABS	3rd	Module Absent, connected to VeeT or VeeR in the module			
7	LVTTL-I	RSo	3rd	Rate Select 0, optionally controls SFP+ module receiver. When high input signaling rate $> 4.25$ GBd and when low input signaling rate $\le 4.25$ GBd.			
8	LVTTL-0	Rx_LOS	3rd	Receiver Loss of Signal Indication (In FC designated as Rx_LOS and in Ethernet designated as Signal Detect)			
9	LVTTL-I	RS1	3rd	Rate Select 1, optionally controls SFP+ transmitter. When high input signaling rate> 4.25 GBd and when low input signaling rate ≤ 4.25 GBd.			
10		VeeR	1st	Module Receiver Ground			
11		VeeR	1st	Module Receiver Ground			
12	CML-O	RD-	3rd	Receiver Inverted Data Output			
13	CML-O	RD+	3rd	Receiver Non-Inverted Data Output			
14		VeeR	1st	Module Receiver Ground			
15		VccR	2nd	Module Receiver 3.3 V Supply			
16		VccT	2nd	Module Transmitter 3.3 V Supply			
17		VeeT	1st	Module Transmitter Ground			
18	CML-I	TD+	3rd	Transmitter Non-Inverted Data Input			
19	CML-I	TD-	3rd	Transmitter Inverted Data Input			
20		VeeT	1st	Module Transmitter Ground			

**Table 2: SFP+ Module PIN Definition** 

# **Absolute maximum rating**

These values represent the damage threshold of the module. Stress in excess of any of the individual Absolute Maximum Ratings can cause immediate catastrophic damage to the module even if all other parameters are within Recommended Operating Conditions.

Parameters	Symbol	Min.	Max.	Unit
Power Supply Voltage	V <sub>CC</sub>	0	+3.6	V
Storage Temperature	Тс	-40	+85	°C
Operating Case Temperature	Тс	0	+70	°C
Relative Humidity	RH	5	95	%

**Table 3: Absolute Maximum Rating** 



# **Recommended operating environment**

Recommended Operating Environment specifies parameters for which the electrical and optical characteristics hold unless otherwise noted.

Parameter	Symbol	Min.	Typical	Max	Unit
Power Supply Voltage	V <sub>CC</sub>	3.135	3.300	3.465	V
Operating Case Temperature	T <sub>C</sub>	0	25	70	°C

**Table 4: Recommended Operating Environment** 

# **LOW Speed Characteristics**

Parameter	Symbol	Min.	Typical	Max	Unit
Power Consumption			1.2	1.2	W
TV Fault DV LOC	VOL	0		0.4	V
TX_Fault,RX_LOS	VOH	Host_Vcc-0.5		Host_Vcc+0.3	V
TV DIC	VIL	-0.3		0.8	V
TX_DIS	VIH	2.0		VCCT+0.3	V
DCO DC1	VIL	-0.3		0.8	V
RS0,RS1	VIH	2.0		VCCT+0.3	V

## **Electrical characteristics**

Parameter	Conditions	Symbol	Min.	Typical	Max	Unit
Nominal Data Rate		VID		10.3125		Gbps
Supply Voltage		Vcc	3.14		3.46	V
Supply Current		Icc		200	300	mA
Power Dissipation		Р			1	W
Transmitter						
Input differential impedance	2	Rin		100		Ω
Single ended data input swing	3	Vin,pp	90		350	mV
Transmit Disable Voltage	4	VD	2		Vcc	V
Transmit Enable Voltage		VEN	Vee		Vee+ 0.8	V

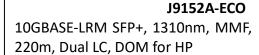


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Receiver						
Termination Mismatch at 1 MHz		ΔΖΜ			5	%
Single Ended Output Voltage Tolerance			-0.3		4.0	V
Output AC Common Mode Voltage					7.5	mV RMS
Output Rise and Fall time (20% to 80%)	5	Tr, Tf	30			Ps
Relative Noise LRM Links with crosstalk	6	dRNx			TBD equati	dB/Hz
Difference Waveform Distortion Penalty	7	dWDP	ре	er SFF-8431		dB
Differential Voltage Modulation Amplitude		VMA	180		600	mV
LOS Fault	8	VLOS fault	2		Vcc HOST	V
LOS Normal	8	VLOS norm	Vee		Vee+ 0.8	V
Power Supply Noise Tolerance	9	VccT/Vcc R	ре	er SFF-8431		mVpp

#### Notes:

- 1. Non-condensing.
- 2. Connected directly to TX data input pins. AC coupling from pins into laser driver IC.
- 3. Per SFF-8431 Rev 3.0
- 4. Into 100 ohms differential termination.
- 5. Measured with Module Compliance Test Board and OMA test pattern.
- 6. Crosstalk source rise/fall time (20%-80%) is 35 ps.
- 7. Defined with reference receiver with 14 T/2 spaced FFE taps and 5 T spaced DFE taps.
- 8. LOS is an open collector output. Should be pulled up with  $4.7k 10k\Omega$  on the host board. Normal operation is logic 0; loss of signal is logic 1. Maximum pull-up voltage is 5.5V.
- 9. As described in Section 2.8.1, SFF-8431 Rev 3.0.





# **General Specifications**

Para	meter	Symbol	Min.	Typical	Max	Unit	Notes
Bit	Rate	BR		10.3125		Gb/sec	1
Bit Err	or Ratio	BER			10-12		2
Maximum Sup	ported Distance	S					
Fiber Type	1310nm OFL Bandwidth						
62.5μm	"FDDI" 160MHz/km	Lmax			220	m	3
υΣ.5μπ	OM1 200MHz/km	Liliax			220	111	3
	400MHz/km				100		
50μm	OM2 500MHz/km	Lmax			220	m	3
	OM3 2000MHz/km				220		

## Notes:

- 1. 10GBASE-LRM
- 2. Tested with a 231 1 PRBS
- 3. Operating range as defined by IEEE standards. Longer reach possible depending upon link implementation.

# **Optical characteristics**

Parameter	Symbol	Min.	Typical	Max	Unit	Notes		
	Transmitter							
Center Wavelength	λt	1260		1355	nm			
	λrms @1260nm			2.4				
RMS spectral width	λrms @ 1260nm-13	-	-	2.4	nm	2		
	λrms @ 1300nm-13			4				
Average Optical Power	Pavg	-6.5	-	0.5	dBm	1		
Extinction Ratio	ER	3.5	-	-	dB			
Optical Modulation Amplitude (OMA)	POMA	-4.5		+1.5	dBm			

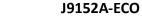


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Peak Launch Power	PMAX			3	dBm	
Transmitter Waveform Dispersion Penalty	TWDP			4.7	dB	3
Average Launch power of OFF transmitter	POFF			-30	dBm	
Uncorrelated Jitter [rms]	Txj			0.033	UI	
Encircled Flux	<5μm	30			%	
Encircled Flux	<11µm	81			70	
Transmitter Reflectance				-12	dB	
Optical Return Loss Tolerance		20			dB	
Relative Intensity Noise	Rin			-128	dB/Hz	
		Receiver				
Comprehensive Stressed	Precursor	-	-	-6.5	dBm	
Receiver Sensitivity (OMA) @	Symmetrica			-6	dBm	5
10.3125Gb/s	Postcursor			-6.5	dBm	
LOS Assert	LosA	-30	-		dBm	
LOS De-assert	LosD			-11	dBm	
Overload	PMAX	-+1.5	-		dBm	4
Receiver Reflectance		-	-	-12	dB	
LOS Hysteresis		0.5			dB	

## Notes:

- 1. Average power figures are informative only, per IEEE802.3aq
- 2. Maximum RMS spectral width as specified by Figure 3
- 3. Optical Eye Mask requires the host board to be SFF-8431 compliant. Optical eye mask per IEEE802.3aq.
- 4. TWDP figure requires the host board to be SFF-8431compliant. TWDP is calculated using the Matlab code provided in clause 68.6.6.2 of IEEE802.3aq
- 5. Receiver overload specified in OMA and under the worst comprehensive stressed condition.
- 6. Conditions of stressed receiver tests per IEEE802.3aq. CSRS testing requires the host board to be SFF-8431 compliant.





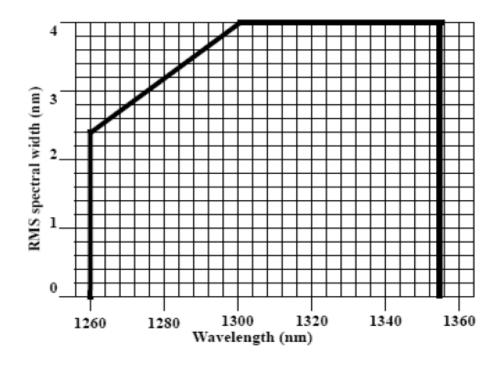


Figure 3
Transmitter Maximum RMS Spectral Width

# **Digital Diagnostic Functions**

The following digital diagnostic characteristics are defined over the Recommended Operating Environment unless otherwise specified. It is compliant to SFF8472 Rev9.2 with internal calibration mode. For external calibration mode please contact our sales stuff.

Parameter	Symbol	Min.	Max	Unit	Notes		
Accuracy							
Transceiver Temperature	DMI_Temp	-3	+3	degC	Over operating temp		
TX Output optical power	DMI_TX	-3	+3	dB			
RX Input optical power	DMI_RX	-3	+3	dB	-3dBm to -12dBm range		
Transceiver Supply voltage	DMI_VCC	-0.08	+0.08	V	Full operating range		
Bias current monitor	DMI_Ibias	-10%	10%	mA			
Dynamic Range Accuracy							



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Transceiver Temperature	DMI_Temp	-5	70	degC
TX Output optical power	DMI_TX	-9	-1	dBm
RX Input optical power	DMI_RX	-18	0	dBm
Transceiver Supply voltage	DMI_VCC	3.0	3.6	V
Bias current monitor	DMI_Ibias	0	16	mA

# **Control and status I/O timing characteristics**

Timing characteristics of control and status I/O are included in Table 8, which is also defined in SFF-8431.

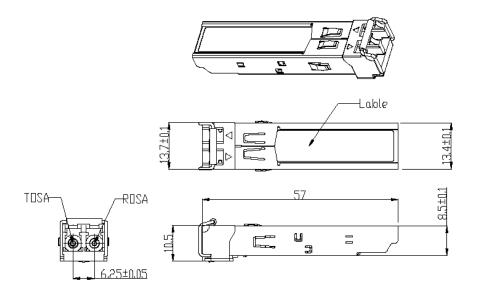
Parameter	Symbol	Min.	Max.	Unit	Conditions
TX_Disable assert time	t_off		100	μs	rising edge of TX_Disable to fall of output signal below 10% of nominal
TX_Disable negate time	t_on		2	ms	Falling edge of Tx_Disable to rise of output signal above 90% of nominal. This only applies in normal operation, not during start up or fault recovery.
Time to initialize 2-wire interface	t_2w_start_up		300	ms	From power on or hot plug after the supply meeting <u>Table 8</u> .
Time to initialize	t_start_up		300	ms	From power supplies meeting Table 8 or hot plug or Tx disable negated during power up, or Tx_Fault recovery, until non-cooled power level I part (or non-cooled power level II part already enabled at power level II for Tx_Fault recovery) is fully operational.
Time to initialize cooled module	t_start_up_cooled		90	s	From power supplies meeting <u>Table 8</u> or hot plug, or Tx disable negated during power up or Tx_Fault recovery, until cooled power level I part (or cooled power level II part during fault recovery) is fully operational.
Time to Power Up to Level II	t_power_level2		300	ms	From falling edge of stop bit enabling power level II until non-cooled module is fully operational
Time to Power Down from Level II	t_power_down		300	ms	From falling edge of stop bit disabling power level II until module is within power level I requirements
TX_Fault assert	TX_Fault_on		1	ms	From occurrence of fault to assertion of TX_Fault
TX_Fault assert for cooled module	TX_Fault_on_coo led		50	ms	From occurrence of fault to assertion of TX_Fault
TX_Fault Reset	t_reset	10		μs	Time TX_Disable must be held high to reset TX_Fault
RS0, RS1 rate select timing for FC	t_RS0_FC, RS1_FC		500	μs	From assertion till stable output
RS0, RS1 rate select timing non FC	t_RS0, t_RS1		10	ms	From assertion till stable output
Rx_LOS assert delay	t_los_on		100	μs	From occurrence of loss of signal to assertion of Rx_LOS
Rx_LOS negate delay	t_los_off		100	μs	From occurrence of presence of signal to negation of Rx_LOS





**Table 8: Timing Characteristics** 

## **Mechanical dimensions:**



### **ESD**

This transceiver is specified as ESD threshold 2kV for all electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

#### **LASER SAFTY**

This is a Class 1 Laser Product according to IEC 60825-1:1993:+A1:1997+A2:2001. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (July 26, 2001)

# **Ordering information**

Part Number	Product Description
J9152A-ECO	1310nm, 10.3125Gpbs, Multi Mode 220m, 0°C ~ +70°C